REMARKS

Claims 1-23 and 47-51 are pending in the present application. Claims 1, 2, 17 and 47 have been amended.

Claim Rejections-35 U.S.C. 102

Claims 1-7, 10-23 and 47-51 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Lee et al. reference (US 2005/0046002). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The stacked semiconductor device of claim 1 includes in combination among other features a first insulating layer "for covering said first insulating material layer of said first multilayer wiring part and provided over the first main surface of said first semiconductor substrate, said first insulating layer is a support member of said first semiconductor substrate"; and a third insulating layer "for covering said second insulating material layer of said second multilayer wiring part and provided over the first main surface of said second semiconductor substrate, said third insulating layer is a support member of said second semiconductor substrate".

As may be readily understood in view of Figs. 12 and 13, manufacturing of the semiconductor device of the present application includes polishing the second main surface (rear surface) of semiconductor substrate 6a to thin the substrate. During the polishing, insulating layer 8a supports substrate 6a. This may be interpreted as

corresponding to the above noted features of claim 1. That is, insulating layer 8a is a supporting member of semiconductor substrate 6a.

The Examiner has interpreted resin encapsulant 41 shown in Fig. 3 of the Lee et al. reference as both the first and second insulating layers of claim 1. That is, resin encapsulant 41 in Fig. 3 of the Lee et al. reference covers both the first main surface and the second main surface of semiconductor chip 11.

However, as described in paragraph [0049] of the Lee et al. reference with respect to Fig. 13, the entirety of the stacked and tested chips and a portion of test wafer 30 are all encapsulated with resin encapsulant 41. This would be understood as sealing the entirety of the device structure, as shown in Figs. 3 and 4. That is, resin encapsulant 41 in Fig. 3 of the Lee et al. reference is not a support member of semiconductor substrate 11 in Fig. 3 of the Lee et al. reference, but in contrast is a sealing member that seals an entirety of the device structure on common substrate 31.

The Lee et al. reference as relied upon thus does not disclose a first insulating layer and a corresponding third insulating layer as would be necessary to meet the features of claim 1. Applicant therefore respectfully submits that the stacked semiconductor device of claim 1 distinguishes over the Lee et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 1-7 and 10-16, is improper for at least these reasons.

The semiconductor device of claim 17 includes in combination among other features a first insulating layer "for covering said insulating layer of said multilayer wiring

part and provided over the first main surface of the said semiconductor substrate, said first insulating layer is a support member of said semiconductor substrate".

As emphasized above, resin encapsulant 41 in Fig. 3 of the Lee et al. reference is a sealing member of the entirety of the structure on common substrate 31. Resin encapsulant 41 is not a support member of substrate 11a, as would be necessary to meet the features of claim 17. Accordingly, Applicant respectfully submits that the semiconductor device of claim 17 distinguishes over the Lee et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 17-23, is improper for at least these reasons.

The semiconductor device of claim 47 includes in combination among other features a first insulating layer "on an uppermost layer of said multilayer wiring part over the first main surface of said semiconductor substrate, said first insulating layer is a support member of said semiconductor substrate".

As emphasized above, resin encapsulant 41 in Fig. 3 of the Lee et al. reference is a sealing member, not a support member of substrate 11a, as would be necessary to meet the features of claim 47. Accordingly, Applicant respectfully submits that the semiconductor device of claim 47 distinguishes over the Lee et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 47-51, is improper for at least these reasons.

Claim Rejections-35 U.S.C. 103

Claims 8 and 9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Lee et al. reference in view of the Murata et al. reference (US 2002/0030266). Applicant respectfully submits that the Murata et al. reference as secondarily relied upon does not overcome the above noted deficiencies of the primarily relied upon Lee et al. reference, and that this rejection of claims 8 and 9 is improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

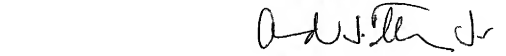
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of two (2) months to March 14, 2010, for the period in which to file a response to the outstanding Office Action. The required fee of $490.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE & WHITT, P.L.L.C.



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